IN THE CLAIMS

Please amend the claims as follows:

1. (Original) An integrated circuit for generating voltages not within a range between a first analog voltage and a second analog voltage, comprising:

an interior division circuit to hold a first amount of charge corresponding to a weighted sum of the first analog voltage and the

second analog voltage based on a digital signal;

an exterior division circuit to hold a second amount of charge corresponding to a difference between the first analog voltage and the second analog voltage; and

an amplifying circuit to generate a voltage corresponding to the sum of the first and second amount of charges.

2. (Currently Amended) The integrated circuit according to claim 1, wherein the first analog voltage is a first differential signal of a first ~~non-inverter~~ non-inverted voltage and a first inverted voltage and the second analog voltage are a second differential signal of a second non-inverted voltage and a second inverted voltage.

3. (Original) The integrated circuit according to claim 1, wherein the amplifying circuit includes a non-inverted input and an inverted input, wherein the non-inverted input is supplied with a first charge corresponding to the sum of the non-inverted voltage of the first analog voltage and the inverted voltage of the second analog voltage, and wherein the inverted input is supplied with a second charge corresponding to the sum of the inverted voltage of the first analog voltage and non-inverted voltage of the second analog voltage.

4. (Original) The integrated circuit according to claim 1, further comprising a selector circuit connected between the exterior division circuit and the amplifying circuit for supplying a charge held by the exterior division circuit or a inverted charge which inverts the charge to the amplifying circuit.

5. (Original) The integrated circuit according to claim 4, wherein the selector circuit further does not supply the charge held by the exterior division circuit to the amplifying circuit.

6. (Original) The integrated circuit according to claim 1, wherein the amplifying circuit includes an amplifier and at least one capacitance element for connecting the input and output of the amplifier.

7. (Original) The integrated circuit according to claim 1, wherein the amplifying circuit includes an amplifier and at least one switch element for connecting the input and output of the amplifier.

8. (Original) The integrated circuit according to claim 1, wherein the interior division circuit comprises a plurality of capacitance elements and a plurality of switch elements.

9. (Original) The integrated circuit according to claim 8, wherein the plurality of capacitance elements are connected to any one of the first analog voltage and the second analog voltage based on the digital signal.

10. (Original) The integrated circuit according to claim 9, wherein the plurality of capacitance elements store the charge in the first period and output a potential corresponding to the charge of the capacitance elements in the second period.

11. (Original) The integrated circuit according to claim 1, wherein the exterior division circuit includes at least one capacitance element and a plurality of switches.

12. (Original) The integrated circuit according to claim 11, wherein the at least one capacitance element accumulates a charge corresponding to the difference of the first analog voltage and the second analog voltage in the first period and outputs a potential corresponding to the charge of the at least one capacitance element in the second period.

13. (Original) The integrated circuit according to claim 1, wherein a plurality of exterior division circuits are provided.

14. (Original) The integrated circuit according to claim 13, wherein at least one of the plurality of exterior division circuits is driven by a control signal.

15. (Original) The integrated circuit according to claim 1, wherein a voltage without the range from the first analog voltage to the second analog voltage is generated.

16. (Original) An A/D converting circuit, comprising:

an interior division circuit to hold a first amount of charge corresponding to a weighted sum of the first analog voltage and second analog voltage based on a digital signal;

an exterior division circuit to hold a second amount of charge corresponding to a difference between the first analog voltage and the second analog voltage; and

an amplifying circuit to generate a voltage corresponding to the sum of the first and second amount of charges.

17. (Original) An A/D converting circuit, comprising:

a first circuit; and

a second circuit;

wherein the first circuit comprises:

a first interior division circuit to hold a first amount of charge corresponding to a weighted sum of the first analog voltage and second analog voltage based on a digital signal;

a first exterior division circuit to hold a second amount of charge corresponding to a difference between the first analog voltage and the second analog voltage; and

a first amplifying circuit to generate a voltage corresponding to the sum of the first and second amount of charges;

wherein the second circuit comprises:

a second interior division circuit to hold a first amount of charge corresponding to a weighted sum of the first analog voltage and second analog voltage based on a digital signal;

a second exterior division circuit to hold a second amount of charge corresponding to a difference between the first analog voltage and the second analog voltage; and

a second amplifying circuit to generate a voltage corresponding to the sum of the first and second amount of charges.

18. (Original) The A/D converting circuit according to claim 17, wherein a voltage without the range from the first analog voltage to the second analog voltage is generated.

19. (Original) The A/D converting circuit according to claim 17, wherein the amplifying circuit includes an amplifier, at least one switch element for connecting the input and output of the amplifier, and at least one capacitance element inserted between the input and output of the amplifier.